IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yuan-Liang Li	Examiner: Renee S. Luebke
Serial No.:	10/090,796	Group Art Unit: 2833
Filed:	March 6, 2002	Docket No: 884.A87US1
Title	SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS	
Assignee:	Intel Corporation	Customer No: 21186

COMMUNICATION RE: SUBMISSION OF UNSIGNED COPIES OF DECLARATIONS

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Charles E. Steffey, certify that the unsigned copies of the Declaration Under 37 C.F.R. 1.131 and Declaration Under 37 C.F.R. 1.132 are identical to the signed copies of said documents. These unsigned copies are provided as a courtesy for purposes of clarity since the text in the signed versions is less than clear.

Respectfully Submitted
YUAN-LIANG LI
By his Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6970

Date: February 24, 2005 By: _____
Charles E. Steffey
Reg. No: 25,179

CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of February 2005.

Name: Christi Hammond Signature: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yuan-Liang Li	Examiner:	Renee S. Luebke
Serial No.:	10/090,796	Group Art Unit:	2833
Filed:	March 6, 2002	Docket No.:	884.A87US1
Title:	SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS		
Assignee:	Intel Corporation	Customer No.:	21186

DECLARATION UNDER 37 C.F.R. § 1.131

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.131 prior to any final rejection of U.S. Patent Application Serial Number 10/090,796 (the "Present Application") to establish invention of the subject matter of the rejected claims of the Present Application prior to June 29, 2001.

I, Yuan-Liang Li, do hereby declare:

1. I have been employed by Intel Corporation from prior to June 29, 2001, to the present. My current job title is Engineering Manager.

2. I am the inventor of the inventive subject matter of the Present Application as described, illustrated, and claimed therein.

3. I am also a co-inventor of the inventive subject matter of U.S. Pat. No. 6,388,207 as described, illustrated, and claimed therein.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and

that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: _____ _____
Yuan-Liang Li

YUAN-LIANG LI
By His Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date _____ By _____
Walter W. Nielsen
Reg. No. 25,539

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment , Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this _____ day of February, 2005.

_____ _____
Name Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yuan-Liang Li	Examiner:	Renee S. Luebke
Serial No.:	10/090,796	Group Art Unit:	2833
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Assignee:	Intel Corporation	Customer No.:	21186

DECLARATION UNDER 37 C.F.R. § 1.132

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.132 prior to any final rejection of U. S. Patent Application Serial Number 10/090,796 (the "Present Application") to establish that the undersigned inventor was a co-inventor of the subject matter disclosed in U.S. Pat. No. 6,495,770.

I, Yuan-Liang Li, do hereby declare:

1. I have been employed by Intel Corporation from prior to December 4, 2000, the filing date of U.S. Pat. No. 6,495,770, to the present. My current job title is Engineering Manager.

2. I am the inventor of the inventive subject matter of the Present Application as described, illustrated, and claimed therein.

3. I am a co-inventor of the inventive subject matter of U.S. Pat. No. 6,495,770 as described, illustrated, and claimed therein, as evidenced by the following:

a. Having earlier conceived the claimed subject matter of U.S. Pat. No. 6,495,770 in the United States with the co-inventors, my name appears along with theirs on two Invention Disclosures, copies of which are attached hereto as Exhibit A (7 pages) and Exhibit B (8 pages).

b. Exhibit A (Paragraph 2) bears the following Concise Title of Invention: "Embedded DC Shunts in Sockets for High Current Applications". The "Date" deleted from page 1 of Exhibit A is prior to December 4, 2000. Other sensitive information has been blocked out from Exhibit A. Figure 22 [sic] of Exhibit A illustrates conceptually a multi-layered socket comprising one or more DC shunts. This is further described in Paragraph 14 on page 5 of Exhibit A.

c. Exhibit B (Paragraph 2) bears the following Concise Title of Invention: "Package DC Shunts for High Power CPU Applications". The "Date" deleted from page 1 of Exhibit B is prior to December 4, 2000. Other sensitive information has been blocked out from Exhibit B. Figure 2 of Exhibit B illustrates conceptually a multi-layered package comprising one or more DC shunts. This is further described in Paragraph 14 on page 5 of Exhibit B.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: _____ _____
Yuan-Liang Li

YUAN-LIANG LI
By His Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date _____ By _____
Walter W. Nielsen
Reg. No. 25,539

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Name

Signature

S/N 10/090,796 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yuan-Liang Li	Examiner:	Renee S. Luebke
Serial No.:	10/090,796	Group Art Unit:	2833
Filed:	March 6, 2002	Docket No.:	884.A87US1
Title:	SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS		
Assignee:	Intel Corporation	Customer No.:	21186

DECLARATION UNDER 37 C.F.R. § 1.131

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P.O. Box 1450
Alexandria, Virginia 22313-1450

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I, Yuan-Liang Li, do hereby declare:

1. I have been employed by Intel Corporation from prior to June 29, 2001, to the present. My current job title is Engineering Manager.

2. I am the inventor of the inventive subject matter of the Present Application as described, illustrated, and claimed therein.

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that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 2-23-05

Yuan-Liang Li

YUAN-LIANG LI
By His Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date 2/23/2005

By Walter W. Nielsen
Walter W. Nielsen
Reg. No. 25,539

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Chris Hammond

Chris Hammond

Name

Signature

S/N 10/090,796

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yuan-Liang Li
Serial No.: 10/090,796
Filed: March 6, 2002
Title: SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS
Assignee: Intel Corporation

Examiner: Renee S. Luebke
Group Art Unit: 2833
Docket No.: 884.A87US1
Customer No.: 21186

DECLARATION UNDER 37 C.F.R. § 1.132

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.132 prior to any final rejection of U. S. Patent Application Serial Number 10/090,796 (the "Present Application") to establish that the undersigned inventor was a co-inventor of the subject matter disclosed in U.S. Pat. No. 6,495,770.

I, Yuan-Liang Li, do hereby declare:

1. I have been employed by Intel Corporation from prior to December 4, 2000, the filing date of U.S. Pat. No. 6,495,770, to the present. My current job title is Engineering Manager.

2. I am the inventor of the inventive subject matter of the Present Application as described, illustrated, and claimed therein.

3. I am a co-inventor of the inventive subject matter of U.S. Pat. No. 6,495,770 as described, illustrated, and claimed therein, as evidenced by the following:

a. Having earlier conceived the claimed subject matter of U.S. Pat. No. 6,495,770 in the United States with the co-inventors, my name appears along with theirs on two Invention Disclosures, copies of which are attached hereto as Exhibit A (7 pages) and Exhibit B (8 pages).

b. Exhibit A (Paragraph 2) bears the following Concise Title of Invention: "Embedded DC Shunts in Sockets for High Current Applications". The "Date" deleted from page 1 of Exhibit A is prior to December 4, 2000. Other sensitive information has been blocked out from Exhibit A. Figure 22 [sic] of Exhibit A illustrates conceptually a multi-layered socket comprising one or more DC shunts. This is further described in Paragraph 14 on page 5 of Exhibit A.

c. Exhibit B (Paragraph 2) bears the following Concise Title of Invention: "Package DC Shunts for High Power CPU Applications". The "Date" deleted from page 1 of Exhibit B is prior to December 4, 2000. Other sensitive information has been blocked out from Exhibit B. Figure 2 of Exhibit B illustrates conceptually a multi-layered package comprising one or more DC shunts. This is further described in Paragraph 14 on page 5 of Exhibit B.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 2-23-05 Yuan-Liang Li

YUAN-LIANG LI
By His Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date 2/23/2005 By Walter W. Nielsen
Walter W. Nielsen
Reg. No. 25,539

DECLARATION UNDER 37 C.F.R. § 1.132
Serial Number: 10/090,795
Filing Date: March 6, 2002
Title: SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS
Assignee: Intel Corporation

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of February, 2005.

Chris Hammond
Name

Chris Hammond
Signature

Merriam-Webster's Collegiate® Dictionary

ELEVENTH EDITION

Merriam-Webster, Incorporated
Springfield, Massachusetts, U.S.A.

A GENUINE MERRIAM-WEBSTER

The name *Webster* alone is no guarantee of excellence. It is used by a number of publishers and may serve mainly to mislead an unwary buyer.

Merriam-Webster™ is the name you should look for when you consider the purchase of dictionaries or other fine reference books. It carries the reputation of a company that has been publishing since 1831 and is your assurance of quality and authority.

First Printing 2003

Library of Congress Cataloging in Publication Data

Merriam-Webster's collegiate dictionary. — Eleventh ed.
p. cm.
Includes index.
ISBN 0-87779-807-9 (Laminated unindexed : alk. paper). — ISBN 0-87779-808-7 (Jacketed hardcover unindexed : alk. paper). — ISBN 0-87779-809-5 (Jacketed hardcover with CD-ROM : alk. paper). — ISBN 0-87779-810-9 (Leatherlook with CD-ROM : alk. paper). — 0-87779-813-3 (Canadian). — 0-87779-814-1 (international).
1. English language—Dictionaries. I. Title: Collegiate dictionary. II. Merriam-Webster, Inc.
PE1628.M36 2003
423—dc21 2003003674
CIP

Made in the United States of America

12TT:QWV03

3. Is often used before introductory expressions such as *for example, that is,* and *namely*.

We were fairly successful; that is, we made our deadlines and met our budget.

4. Separates phrases or items in a series when they contain commas.

The assets include $22 million in land, buildings, and equipment; $34 million in cash and investments; and $8 million in inventory.

The Pissarro exhibition will travel to Washington, D.C.; Manchester, N.H.; Portland, Ore.; and Oakland, Cal.

The votes against were: Precinct 1, 418; Precinct 2, 332; Precinct 3, 256.

5. Is placed outside quotation marks and parentheses.

They again demanded "complete autonomy"; the demand was again rejected.

She found him urbane and entertaining (if somewhat overbearing); he found her charmingly ingenuous.

/ Slash

1. Separates alternatives, usually representing the words *or* or *and/or*.

alumni/ae his/her

2. Replaces the word *to* or *and* in some compound terms and ranges.

1998/99 *or* 1998–99

the May/June issue *or* the May–June issue

3. Separates lines of poetry that are run in with the text. A space usually precedes and follows the slash.

In Pope's words: "'Tis with our judgments as our watches, none / Go just alike, yet each believes his own."

4. Separates the elements in a numerical date, and numerators and denominators in fractions.

on 9/11/01 a 7/8-mile course

5. Represents the word *per* or *to* when used between units of measure or the terms of a ratio.

400,000 tons/year price/earnings ratio

29 mi/gal 20/20 vision

6. Punctuates some abbreviations.

w/o [*for* without] I/O [*for* input/output]

c/o [*for* care of] P/E [*for* price/earnings]

7. Punctuates Internet addresses.

http://unabridged.Merriam-Webster.com/

Foreign Marks

1. Guillemets « » often enclose quotations in French and other European languages.

Marie Antoinette est censée dire «qu'ils mangent de la brioche».

2. Spanish exclamation points ¡ ! are used in pairs to enclose an exclamatory sentence in Spanish writing.

¡Qué buen día!

3. Spanish question marks ¿ ? are used in pairs to enclose an interrogatory sentence in Spanish writing.

¿Qué es esto?

TMG INVENTION DISCLOSURE, Rev 3, 8/99
Located at: http://legal.intel.com

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call

Fill out the below and follow the instructions:

1. Field of the Invention:

- ☐ Semiconductor Process: device and integration
- ☐ Semiconductor Process + Equipment: thin films
- ☐ Semiconductor Process + Equipment: etch/litho
- ☐ Circuit Design
- ☐ Flash
- ☐ Test
- ☐ CQN (Q&R)
- ☐ Packaging
- ☐ Boards/Cartridge
- ☐ Automation
- ☒ Other

RECEIVED

PATENT DATABASE GROUP
INTEL LEGAL TEAM

2. Concise Title of Invention:
Embedded DC Shunts in Sockets for High Current Applications

3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The invention is:
A New Design to split DC & high frequency currents through sockets.

The key elements are:

1. **Large pieces of metal are embedded in a socket to provide a shunt for DC current to flow.**
2. **Metal pieces are created on 1,2,3, or 4 sides of a socket to provide a shunt for DC current to flow.**

4. Inventor(s):

Name: Yuan-Liang Li
E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: Taiwan | Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG | Contractor: | Inventor Signature:

Division Name:
ATD_x__ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD____TCAD___
Other?_____

YES _____

NO ___x____

Name: David G. Figueroa

E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: USA | Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG | Contractor: | Inventor Signature:

Division Name:
ATD_x__ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD____TCAD___
Other?_____

YES _____

NO ___x____

Name: PR Patel

E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: USA | Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG | Contractor: | Inventor Signature:

Division Name:
ATD_X_ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD____TCAD___
Other?_____

YES _____

NO ___X___

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: _____
SUPERVISOR NAME: PR Patel _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date:

(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? No.
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale? No
If yes, explain and give date:

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? No If yes, give contract name and number:

10. Explain the problem being addressed by the invention:
The problem being addressed by this invention is high current through sockets. High currents through sockets require low resistances to have a small power dissipation as described by, Power = Current squared x Resistance. Larger power dissipations in the socket result in higher temperatures in the socket.

11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by:
This problem of increasing currents through sockets to supply the high currents to higher power CPU's is currently solved by increasing the number of pins, which lowers the total resistance and results in a lower power dissipation. This is costly not only in terms of actual dollar cost for the extra pins, but also for the real estate needed for the extra pins.

12. Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is:
This invention provides DC shunts that will provide a path for 90% of the total current. This moves the high DC current away from pins. By doing this, the power dissipation through the pins is decreased to about 90%, which is expected to remove reliability concerns that involve heat. Because of the extreme currents of Intel's future high power CPU's, this is an expected need. Without this invention, self heating and resulting reliability issues are expected as the number of pins needed are greater than the number than can be supplied in a cost-effective socket

13. Is the invention experimentally verified?
a. Is the invention verified with simulation?

b. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

Referenced sketches/dwg's/diagrams: (use additional page(s))

As the frequencies of Intel processors increase, the currents required increases proportionally. In addition, while the magnitude of the current increases, the amount of area to carry the current through the socket is decreased. The problem being addressed by this invention is high current through sockets. High currents through sockets require low resistances to have small power dissipation as described by, Power = Current squared times the Resistance. Larger power dissipations in the socket result in higher temperatures in the socket, and higher temperatures are expected to cause problems quality and reliability.

The problem of increasing currents through sockets to supply the high currents to higher power CPU's is currently solved by increasing the number of pins, which lowers the total resistance and results in a lower power dissipation. A picture of these pins is shown in Figure 1. This is costly not only in terms of actual dollar cost for the extra pins, but also for the real estate needed for the extra pins. In addition, if the number of pins added for power dissipation doesn't provide a much lower resistance than the resistance of the pins in the core region, the effectiveness of the additional pins may not sufficiently reduce the current flowing through one region of the package. In other words, additional pins must provide an effective DC shunt.

This invention provides very effective DC shunts that will provide a path for 90% of the total current. This moves the high DC current away from pins. By doing this, the power dissipation through the pins is decreased to about 90%, which is expected to remove reliability concerns that involve heat. Because of the extreme currents of Intel's future high power CPU's, this is an expected need. Without this invention, self-heating and resulting reliability issues are expected as the number of pins needed are greater than the number than can be supplied in a cost-effective socket.

In Figure 2, this invention is implemented by inserting metals into sockets. This method can be achieved using 1, 2, 3, or 4 sides of the socket, with 1 or more side terminals per side, or creating shunts internal the socket. This can be implemented by providing 1 or more shunts through a socket.

15. Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

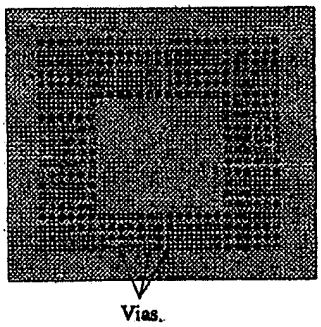

Figure 1. Present State of the Art

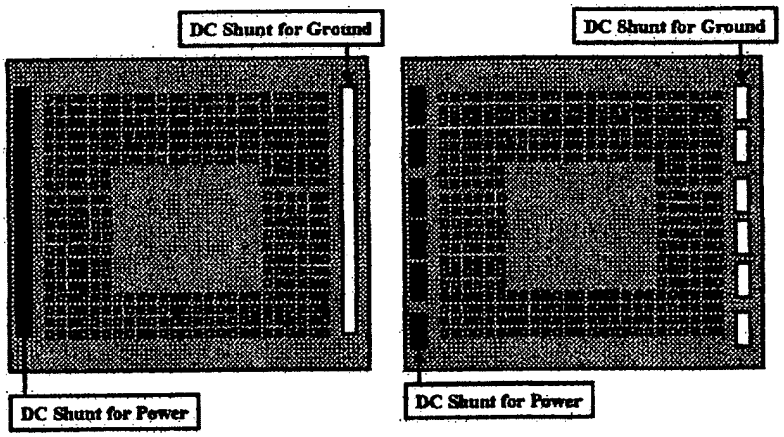

Figure 22. DC Shunts Embedded in Sockets

Fabrication

16. **Key Supporting Data (1 page limit on separate page):**
    99 % current flows in DC shunt.

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):**

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____**

19. **Any other information IP committee should consider?**

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers
Semiconductor Process – etch/litho (etch),	John Carruthers, Peter Silverman, Peter Charvat Yan Borodovsky (litho)
Circuit Design Galivanche	Ian Young, Greg Taylor, Clair Webb, Rajesh
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R) Carruthers,	Ian Young, Greg Taylor, Clair Webb, John Valluri (Bob) Rao, Naomi Obinata
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys Greaves	Ray Werner, Rob Winkle, Naomi Obinata, John

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
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Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers
Semiconductor Process – etch/litho (etch),	John Carruthers, Peter Silverman, Peter Charvat Yan Borodovsky (litho)
Circuit Design Galivanche	Ian Young, Greg Taylor, Clair Webb, Rajesh
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R) Carruthers,	Ian Young, Greg Taylor, Clair Webb, John Valluri (Bob) Rao, Naomi Obinata
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys Greaves	Ray Werner, Rob Winkle, Naomi Obinata, John

TMG INVENTION DISCLOSURE, Rev 3, 8/99
Located at: http://legal.intel.com

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call

Fill out the below and follow the instructions:

1. Field of the Invention:

- ☐ Semiconductor Process: device and integration
- ☐ Semiconductor Process + Equipment: thin films
- ☐ Semiconductor Process + Equipment: etch/litho
- ☐ Circuit Design
- ☐ Flash
- ☐ Test
- ☐ CQN (Q&R)
- ☒ Packaging
- ☐ Boards/Cartridge
- ☐ Automation
- ☐ Other

2. Concise Title of Invention:
Package DC Shunts for High Power CPU Applications

3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The invention is:
A New Design to split DC & high frequency currents through packages.

The key elements are:

1. **Large pieces of metal are integrated with the package (include the following, but not limited to FCPGA, OLGA, Ceramic) from the top of the package to the bottom of the package to provide a shunt for DC current to flow.**
2. **Metal pieces are created on 1,2,3, or 4 sides of a package to provide a shunt for DC current to flow.**
3. **Large pieces of metal are created internal to the package to provide a shunt for DC current to flow.**

4. Inventor(s):

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E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: Taiwan | Supervisor Name: | Supervisor Phone: | Supervisor M/S:
Group Name: TMG | Contractor: | Inventor Signature:
Division Name:
ATD_x_ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD___TCAD___
Other?_____
YES _____
NO ___x____

Name: David G. Figueroa

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Citizenship: USA | Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG | Contractor: | Inventor Signature:
Division Name:
ATD_x_ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD___TCAD___
Other?_____
YES _____
NO ___x____

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Citizenship: USA | Supervisor Name: | Supervisor Phone: | Supervisor M/S:

Group Name: TMG | Contractor: | Inventor Signature:
Division Name:
ATD_X_ PTD___ CTM___
CR___ STTD___ CQN ___
SMTD___TCAD___
Other?_____
YES _____
NO ___X___

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: _____
SUPERVISOR NAME: PR Patel_____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date:

(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? No.
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale? No
If yes, explain and give date:

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? No If yes, give contract name and number:

10. Explain the problem being addressed by the invention:
The problem being addressed by this invention is high current through packages. High currents through packages require low resistances to have a small power dissipation as described by, Power = Current squared x Resistance. Larger power dissipations in the package result in higher temperatures in the package.

11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by:
This problem of increasing currents through packages to supply the high currents to higher power CPU's is currently solved by increasing the number of vias vertically through the package, which lowers the total resistance and results in a lower power dissipation. This is costly not only in terms of actual dollar cost for the extra vias, but also for the real estate needed for the extra vias.

12. Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is:
This invention provides DC shunts that will provide a path for 90% of the total current. This moves the high DC current away from vias that are critical to lowering the inductance through the package. By doing this, the power dissipation through the vias is decreased to about 90%, which is expected to remove reliability concerns that involve heat. Because of the extreme currents of Intel's future high power CPU's, this is an expected need. Without this invention, self heating and resulting reliability issues are expected as the number of vias needed are greater than the number than can be supplied in a cost-effective package

13. Is the invention experimentally verified? No
a. Is the invention verified with simulation? yes

b. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

Referenced sketches/dwg's/diagrams: (use additional page(s))

As the frequencies of Intel processors increase, the currents required increases proportionally. In addition, while the magnitude of the current increases, the amount of area to carry the current through the package is decreased. The problem being addressed by this invention is high current through packages. High currents through packages require low resistances to have small power dissipation as described by, Power = Current squared times the Resistance. Larger power dissipations in the package result in higher temperatures in the package, and higher temperatures are expected to cause problems quality and reliability.

The problem of increasing currents through packages to supply the high currents to higher power CPU's is currently solved by increasing the number of vias vertically through the package, which lowers the total resistance and results in a lower power dissipation. A picture of these vias is shown in Figure 1. This is costly not only in terms of actual dollar cost for the extra vias, but also for the real estate needed for the extra vias. In addition, if the number of vias added for power dissipation doesn't provide a much lower resistance than the resistance of the vias in the core region, the effectiveness of the additional vias may not sufficiently reduce the current flowing through one region of the package. In other words, additional vias must provide an effective DC shunt.

This invention provides very effective DC shunts that will provide a path for 90% of the total current. This moves the high DC current away from vias that are critical to lowering the inductance through the package. By doing this, the power dissipation through the vias is decreased to about 90%, which is expected to remove reliability concerns that involve heat. Because of the extreme currents of Intel's future high power CPU's, this is an expected need. Without this invention, self-heating and resulting reliability issues are expected as the number of vias needed are greater than the number than can be supplied in a cost-effective package.

In Figure 2, this invention is implemented by creating side terminals on packages. This method can be achieved using 1, 2, 3, or 4 sides of the package, with 1 or more side terminals per side, or creating shunts internal to the package. This can be implemented by providing 1 or more shunts through a package.

15. Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

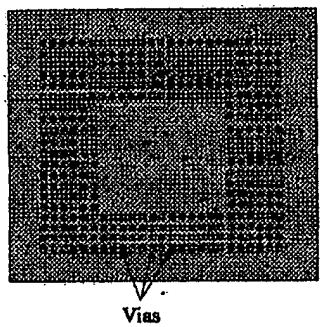

Figure 1. Present State of the Art

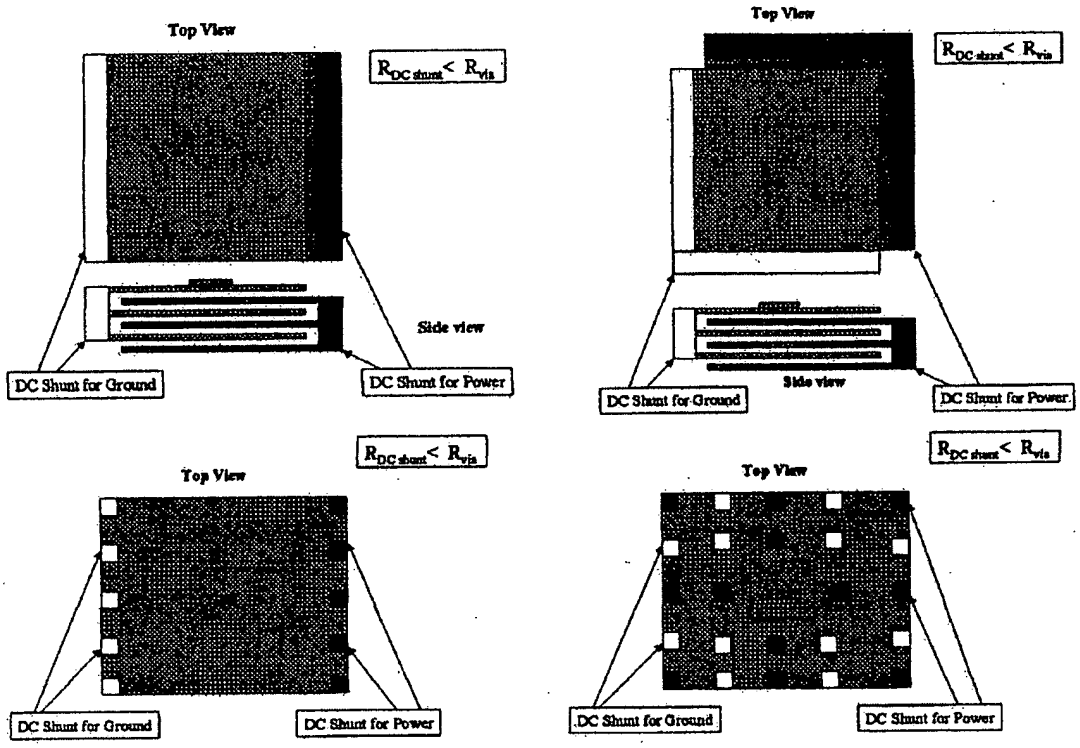

Figure 2. DC Shunts in Packages

Fabrication

16. Key Supporting Data (1 page limit on separate page):
99% current flows in DC shunt.

16. **Key Supporting Data (1 page limit on separate page):**
99% current flows in DC shunt.

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):**

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____**

19. **Any other information IP committee should consider?**

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers
Semiconductor Process – etch/litho (etch),	John Carruthers, Peter Silverman, Peter Charvat Yan Borodovsky (litho)
Circuit Design Galivanche	Ian Young, Greg Taylor, Clair Webb, Rajesh
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R) Carruthers,	Ian Young, Greg Taylor, Clair Webb, John

	Valluri (Bob) Rao, Naomi Obinata
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys	Ray Werner, Rob Winkle, Naomi Obinata, John Greaves